Infineon

Software-Defined Radio Project

A Baseband Processor Architecture for Multi-Standard Cell Phones

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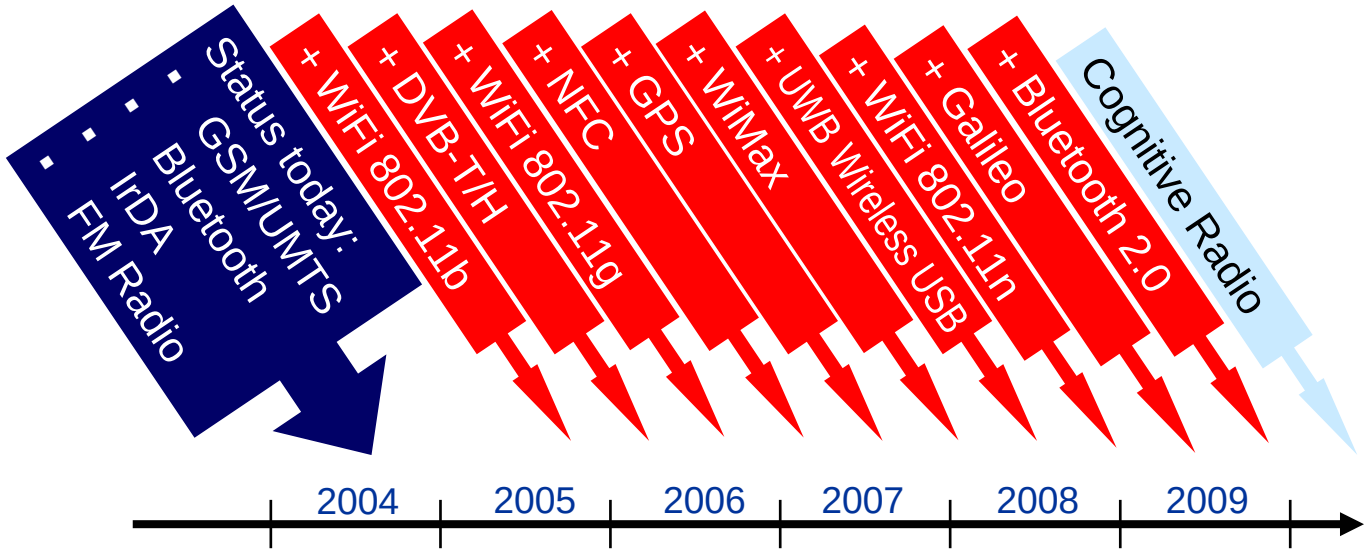
Never stop thinking.

Trend for Cell Phones



Future Cell Phones are Multi-Standard !

- Cellular
- WLAN
- Broadcast
- Positioning
- PAN

What is the best architecture ?

Outline

- Motivation & Challenges
- Levels of Parallelism and Analysis of Baseband Requirements
- MuSIC Hardware Architecture
- Software Architecture & Tools
- Summary and Outlook

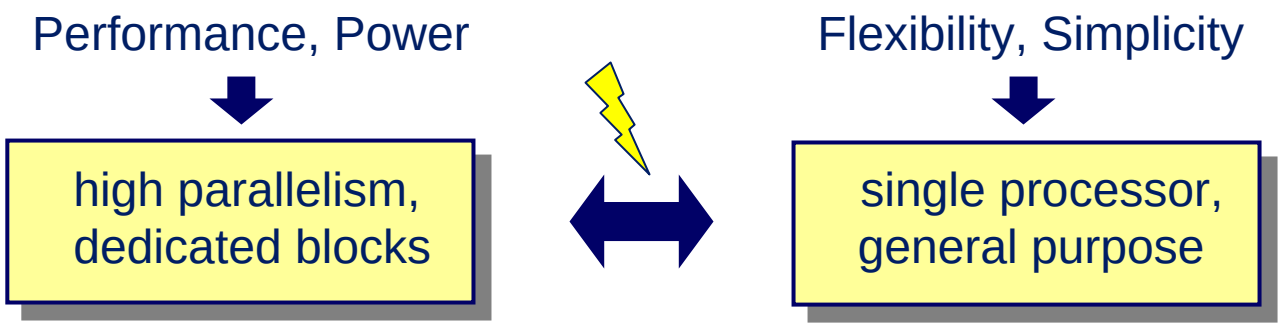
Multi Standard Cell Phone Requirements

- More flexibility and scalability necessary for baseband processing
  - Variety of existing and evolving standards
  - Diversification of products
  - Time to market
  - NRE Costs
  - ⇨ one common **platform** for all regions and product classes
- Easy-to-program solution
- Efficiency (Power, Area)
- Standards to be supported in first prototype (some concurrently)
  - UMTS FDD at 384 kb/s
  - CDMA2000 1x DV
  - GSM/GPRS/EDGE class 12
  - IEEE 802.11b / g (802.11g with reduce data rate)
  - Bluetooth
  - DAB
  - GPS

⇨ Baseband Processor Architecture with Reconfigurable RF Front-End

Architecture Challenge for the Baseband Processor

- Baseband performance required: **10'000+ MIPS** equivalents
- Power budget: **200 mW** for UMTS
- Maximum flexibility
- Simplicity of programming model

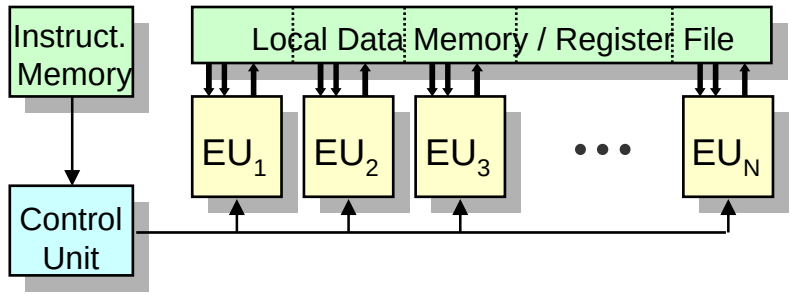


⇨ Strategy:

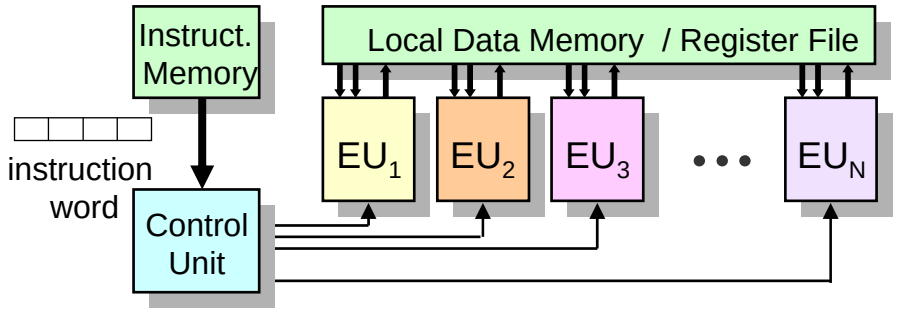
Search for most flexible architecture that meets power constraints !

The Different Levels of Parallelism to Exploit

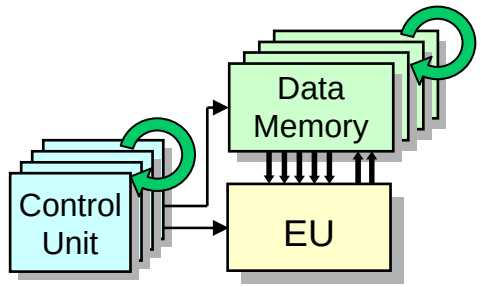
- Data Level Parallelism
  - Inherent in most BB alg.'s
  - SIMD Architecture
    - High Efficiency
    - Compiler issues
    - Amdahl's Law !



- Instruction Level Parallelism
  - VLIW Architecture
    - Compiler friendly
    - Register file issues
  - Complex Instructions

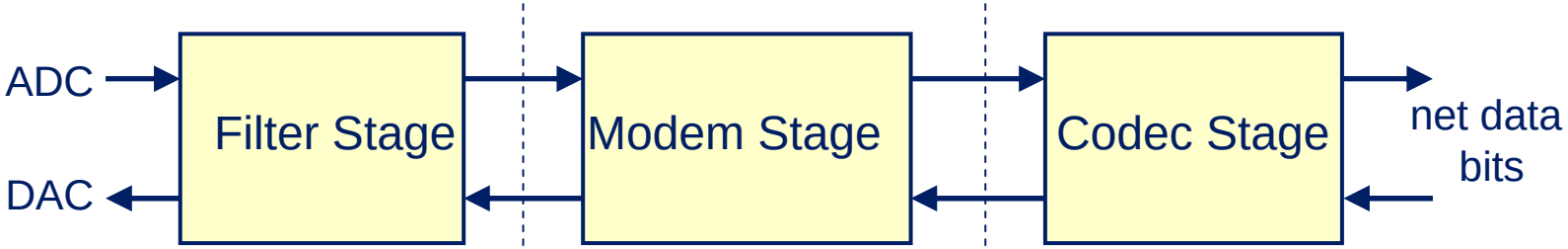


- Task Level Parallelism
  - Multiple Interleaved Threads
    - Relaxed Memory Requirements
    - Increased Latency
  - Multiple Processors Core
    (ASIPs, Coprocessors, Accelerators)



Best Results By Exploiting All Levels Of Parallelism !

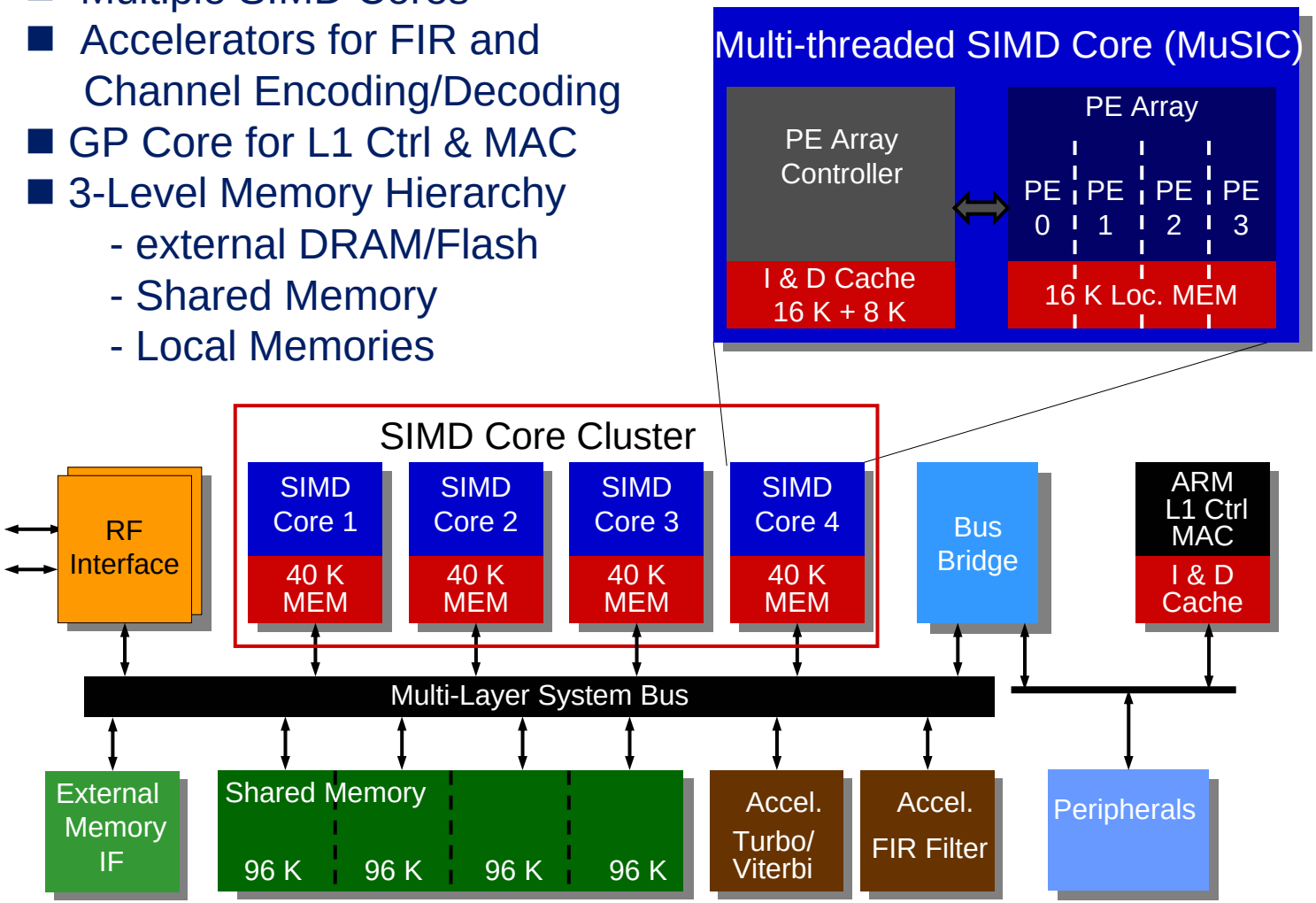
Baseband Processor Stages: Different Requirements



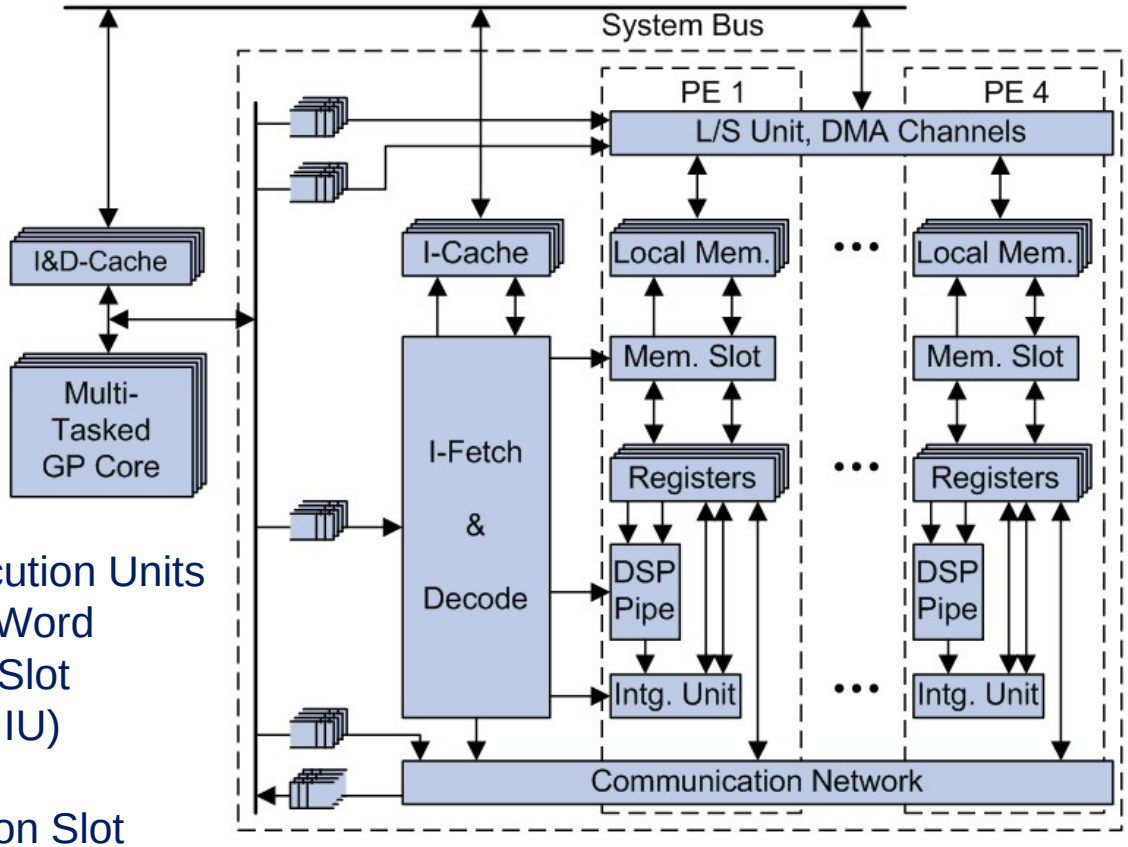
Filter Stage	Modem Stage	Codec Stage
■ Filter Operation – signal shaping – band limitation – rate conversion	■ Modulation / Demodulation – equalizing – synchronization – QAM, PSK, … – CDMA, TDMA, … – MIMO	■ Encoding/Decoding – (de)interleaving – (de)puncturing – Viterbi, turbo, – rate matching, …
➢ high processing power ➢ fixed by standard	➢ high proc. power ➢ complex algorithms ➢ high flexibility ➢ control & dataflow	➢ moderate processing power ➢ complex algorithms ➢ determined by standard
⇨ application specific accelerator (Programmable Filter)	⇨ **Processor Solution**	⇨ application specific accelerator (Turbo-Viterbi Processor)

Infineon Baseband Processor Architecture MuSIC

- Multiple SIMD Cores
- Accelerators for FIR and Channel Encoding/Decoding
- GP Core for L1 Ctrl & MAC
- 3-Level Memory Hierarchy
  - external DRAM/Flash
  - Shared Memory
  - Local Memories

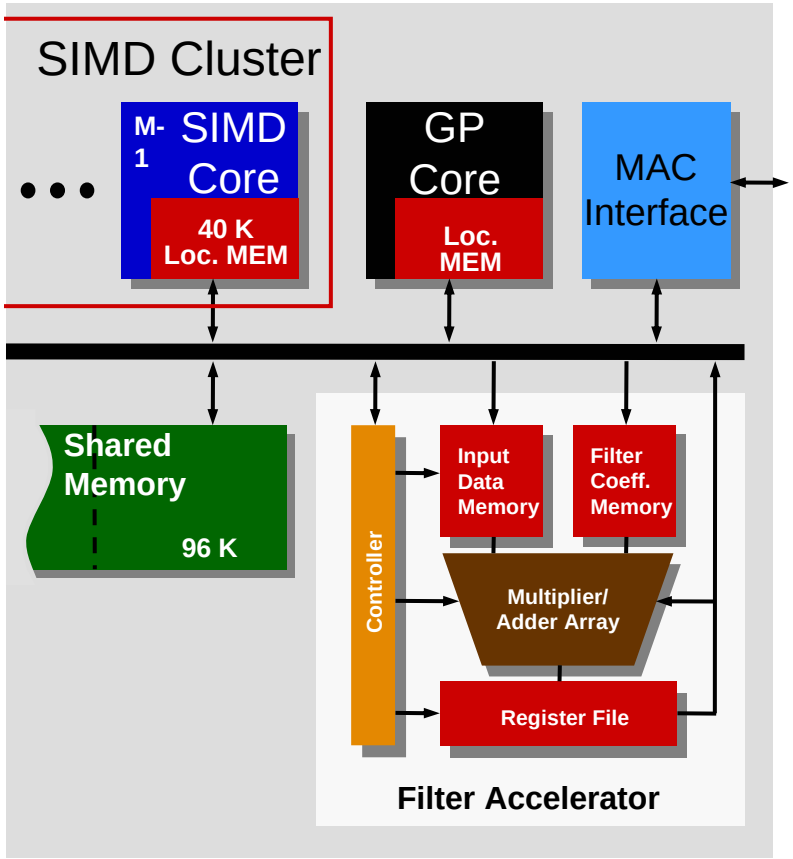


Block Diagram of Multi-Threaded SIMD Core



- 4-way SIMD Execution Units
- Long Instruction Word
  - Computation Slot (DSP Pipe & IU)
  - Memory Slot
  - Communication Slot
- 4 Interleaved Threads
- Multi-tasked GP core to control the SIMD core
- Local Data Memories instead of L1 Cache

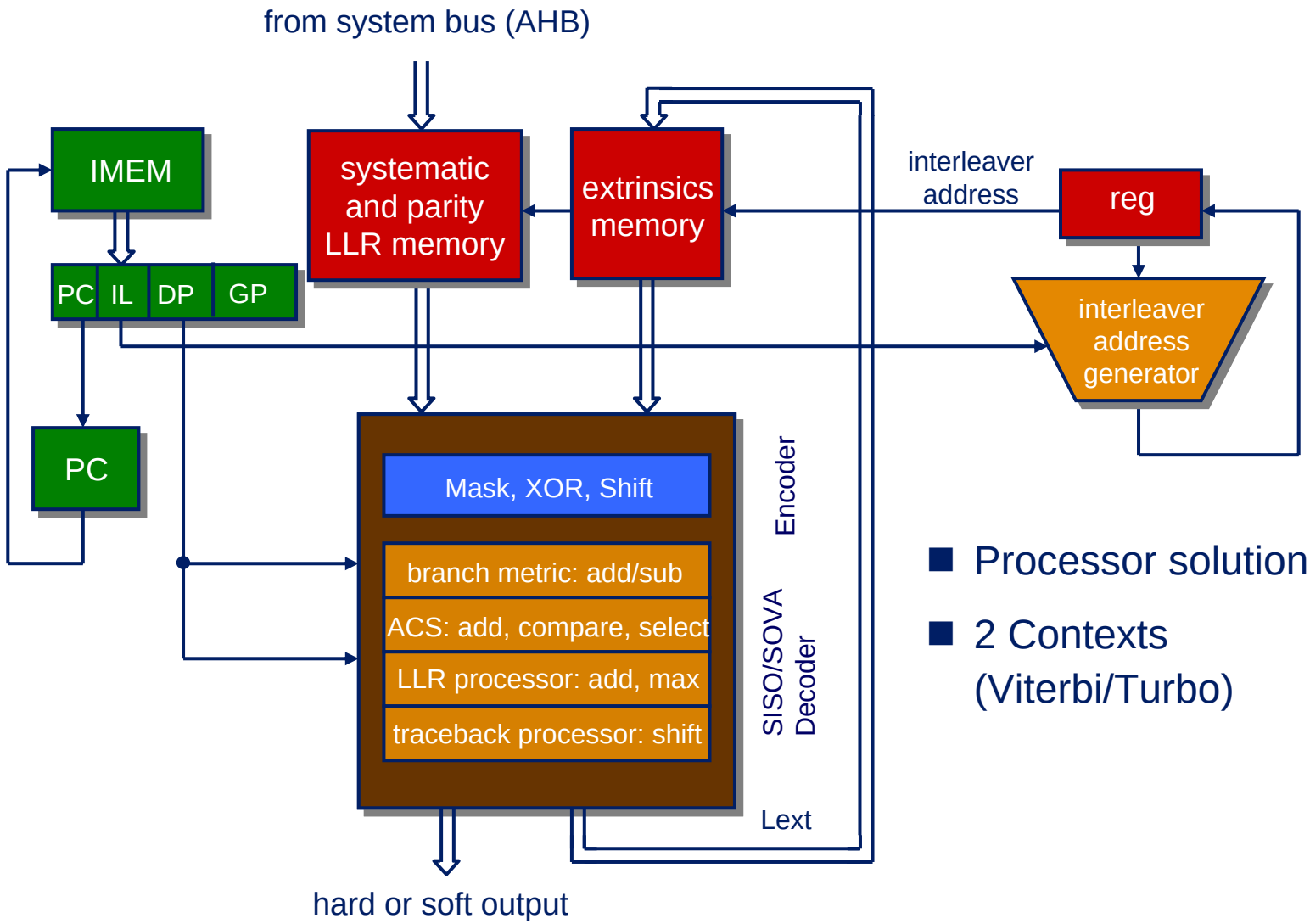
SDR Filter Accelerator



- Configurable Coprocessor
- Multi-threaded (4 contexts)
- Complex filter (I/Q)

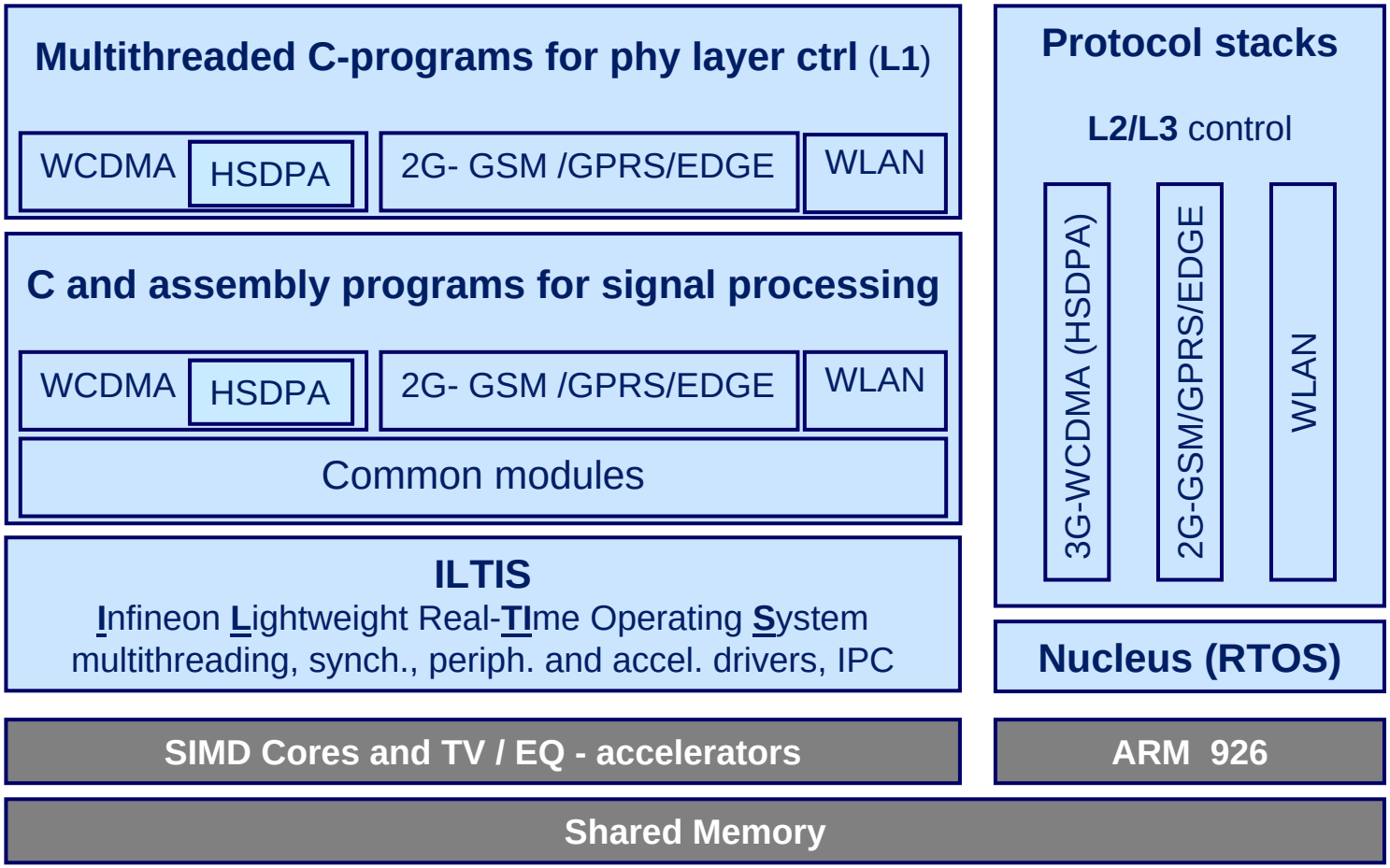
	filter length	data word length	coeff. word length	sample rate
WCDMA	approx. 20	approx. 8	8..10	7.68 MHz
WLAN 802.11	15	10..12	10..12	22/40 MHz

SDR Channel Coding Processor

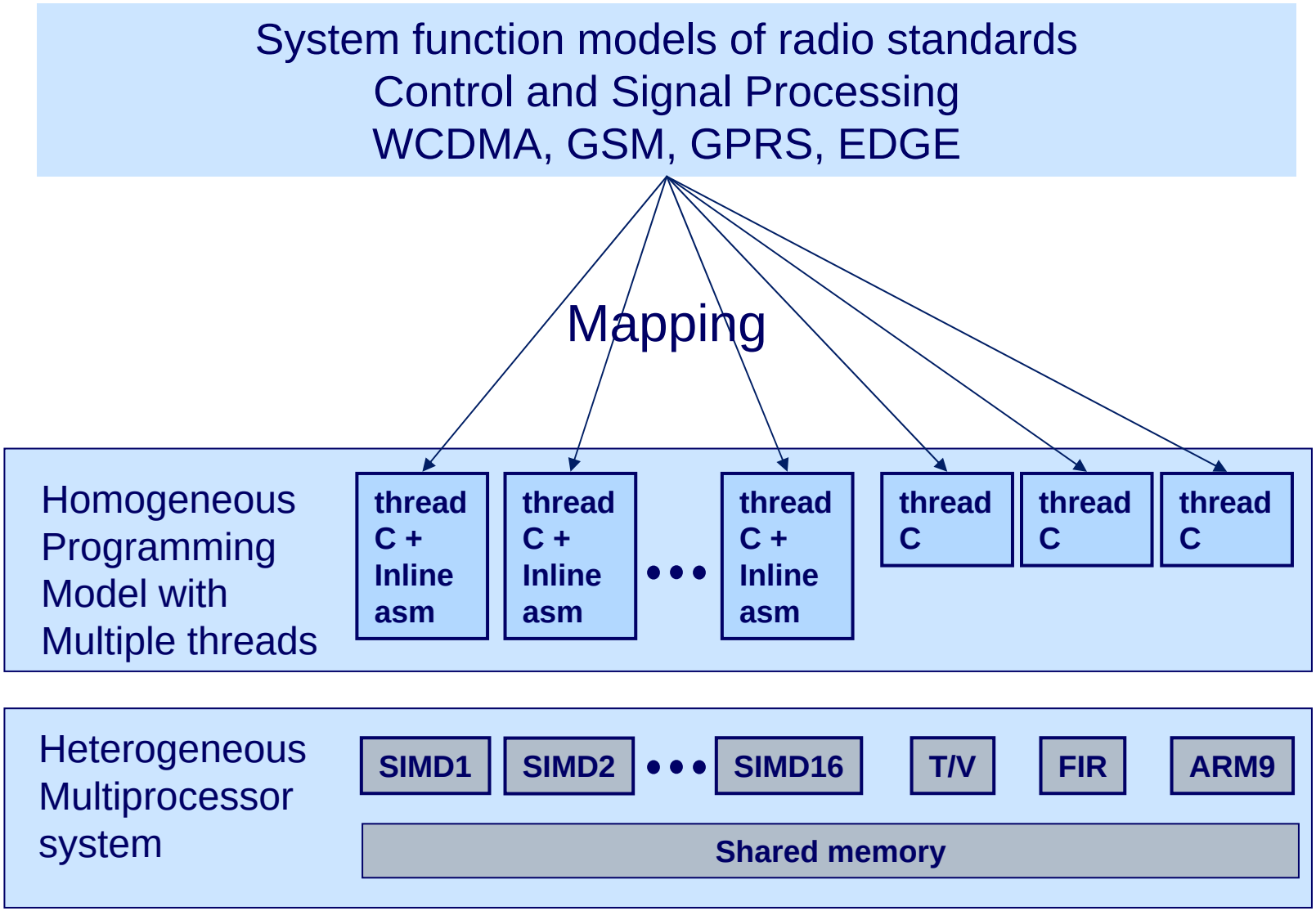


- Processor solution
- 2 Contexts (Viterbi/Turbo)

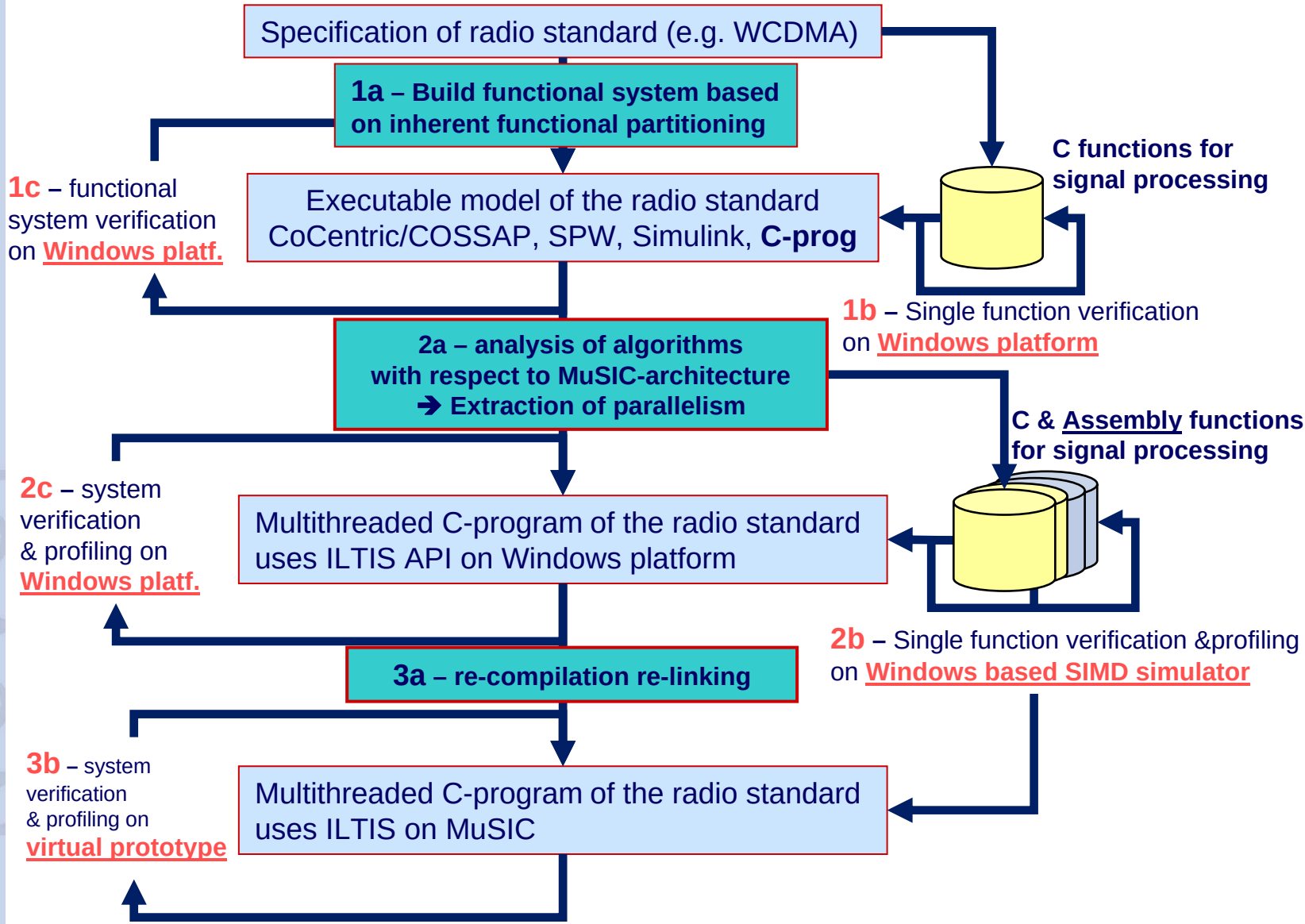
Baseband Software Architecture



Programming Model



Software Design Process



Tools

High-Level System Modelling

Simulink (MathWorks)	**MLDesigner** (ML Design Technologies)	**Metropolis/Ptolemy** (UC Berkeley)
Extensions Converter (IFX)	**CoCentric (COSSAP)** (Synopsys)	**SPW** (CoWare)

Code Generation

Partitioning/Scheduling (IFX)

Ctrl Code Generation (IFX)

Eclipse (IBM)

ILTIS alpha (IFX)	**RC1632 Compiler** (IFX)	**SIMD Compiler** (IFX)	**ARMCC** (ARM)	**Nucleus** (Mentor)

SystemC Virtual Prototype (CoCentric System Studio)

RC1632 Simulator (IFX with LisaTek/CoWare)	**SIMD Simulator** (IFX)	**ARMulator** (ARM)
SIMD Cores and TV / EQ - accelerators		**ARM 926**

Shared Memory / System-Bus

Summary & Outlook

- Future multi-standard cell phones require flexible baseband processing
- Power-efficient and flexible solution based on parallel LIW-SIMD processors combined with accelerators
- Software development framework for multi-threaded programs
- Infineon’s SDR platform offers versatility and scalability beyond today's cell phone standards
- Profiling results show feasibility of approach
- Status and outlook
  - Virtual prototype of platform available
  - Platform demonstrator in Q1 2006

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Thanks for your attention !

Questions ?

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